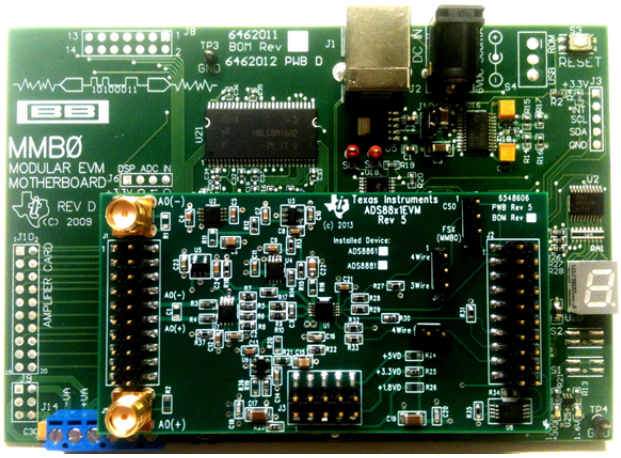
ADS8861EVM-PDK



ADS8861EVM-PDK

This user's guide describes the operation and use of the ADS8861 evaluation module (EVM). The ADS8861 is an 16-bit, true-differential, unipolar, successive approximation register (SAR), analog-to-digital converter (ADC) with a maximum throughput of 1 MSPS. This ADC is very low power with excellent noise and distortion performance for ac or dc signals. The performance demonstration kit (PDK) eases EVM evaluation with additional hardware and software for computer connectivity through universal serial bus (USB). The ADS8861EVM-PDK includes the ADS8861EVM as a daughter card, MMB0 motherboard, A-to-B USB cable, and 6-V wall-adapter power supply. This user's guide covers the circuit description, schematic diagram, and bill of materials for the ADS8861EVM daughter card.

The related documents shown in Related Documentation are available for download at www.ti.com.

Related Documentation

Device	Literature Number
ADS8861	SBAS557
REF5045	SBOS410
OPA333	SBOS351
OPA330	SBOS432
THS4281	SLOS432
THS4521	SBOS458
TPS78833	SLVS382

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1 ADS8861EVM-PDK Overview

The ADS8861EVM is an evaluation module built to the TI modular EVM system specifications. The EVM by itself does not have a microprocessor and cannot run software. Thus, the EVM is available as part of the ADS8861EVM-PDK kit that combines the ADS8861EVM as a daughter board with the DSP-based MMB0 motherboard using ADCPro™ software as a graphical user interface (GUI).

ADCPro software collects, records, and analyzes data from ADC evaluation boards. ADCPro runs different plug-in programs to easily expand testing and data collection capabilities. In combination with the ADS8861EVM plug-in program, ADCPro offers a comprehensive evaluation environment for the ADS8861. For more details on ADCPro, see the *ADCPro Analog-to-Digital Converter Evaluation Software User's Guide* (SBAU128), available for download from www.ti.com.

ADS8861EVM Daughter Board Features:

- Includes support circuitry as a design example to match ADC performance
- 3.3-V slave serial peripheral interface (SPI)
- Serial interface header for easy connection to TI DSP-based communication systems
- Compatible with the TI modular EVM system
- Designed for 5-V analog supply
- Onboard 4.5-V voltage reference
- Bipolar (–4.3 V to 4.3 V) or unipolar (0 V to 8.6 V) input range
- Allows single-ended or differential input signals

ADS8861EVM-PDK Kit Additional Features:

- USB port for computer interfacing
- Regulated 5-V and 3.3-V supplies for powering the EVM daughter board
- Easy-to-use evaluation software for Windows® operating systems
- Data collection to text files
- Built-in analysis tools including scope, FFT, and histogram displays
- Easily expandable with new analysis plug-in tools from Texas Instruments

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2 EVM Analog Interface

The ADS8861EVM is designed for easy interfacing to multiple analog sources. SMA connectors allow the EVM to have input signals connected through coaxial cables. In addition, the Samtec™ connector provides a convenient 10-pin, dual-row, header and socket combination at J1. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. All analog inputs are buffered by the THS4521 high-speed, fully-differential amplifier in order to properly drive the ADS8861 ADC inputs.

Use appropriate caution when handling these pins. Table 1 summarizes the pinout for the analog interface J1.

Table 1. J1: Analog Interface Pinout (Samtec 10 x 2)

Pin Number	Signal	Description
J1.10	A0(–)	Channel 0 negative differential input. This pin can be grounded for single-ended signals.
J1.12	A0(+)	Channel 0 positive differential input or input for single-ended signals.

Table 2 lists the SMA analog inputs.

Table 2. SMA Analog Inputs

Pin Number	Signal	Description
J4	A0(–)	Channel 0 negative differential input. This pin can be grounded for single-ended signals.
J5	A0(+)	Channel 0 positive differential input or input for single-ended signals.

2.1 Differential Input Signal Configuration

Although the ADS8861 can only convert unipolar differential signals, bipolar differential signals can be applied at the EVM inputs because the EVM inputs are conditioned by the THS4521 fully-differential amplifier. This EVM sets the THS4521 output common-mode voltage to 2.25 V, corresponding to V_{REF} / 2. Thus, a bipolar differential signal with a common-mode voltage of 0 V can be applied at the EVM inputs A0(–) and A0(+). Then, the THS4521 shifts the common-mode voltage to 2.25 V. Even though the input common-mode voltage can be corrected, the input signals must limit the differential range from –4.3 V to 4.3 V to avoid saturating the amplifier output because the THS4521 is powered by a 5-V supply. Figure 1 shows an input signal with a 0-V common-mode voltage and an 8.6-V differential voltage, where the common-mode voltage is changed from 0 V to 2.25 V.

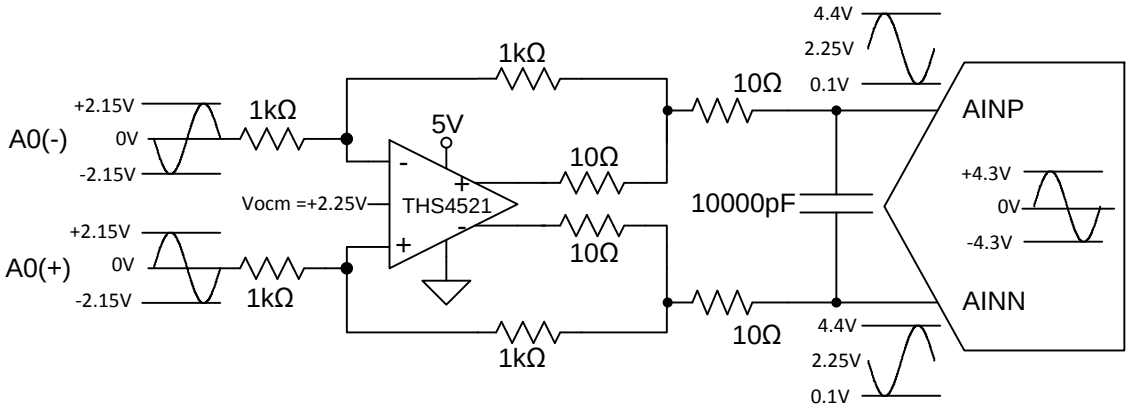


Figure 1. Differential Input Example

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2.2 Single-Ended Signal Configuration

The ADS8861 can only convert single-ended signals between 0 V and V_{REF}. The THS4521 can condition a single-ended signal to a differential signal, thus allowing a larger input voltage range for the EVM input A0(+). The single-ended signal range can be 0 V to 8.6 V or –4.3 V to 4.3 V to avoid saturating the amplifier output. The EVM A0(–) input should be grounded for single-ended signals, as shown in Figure 2.

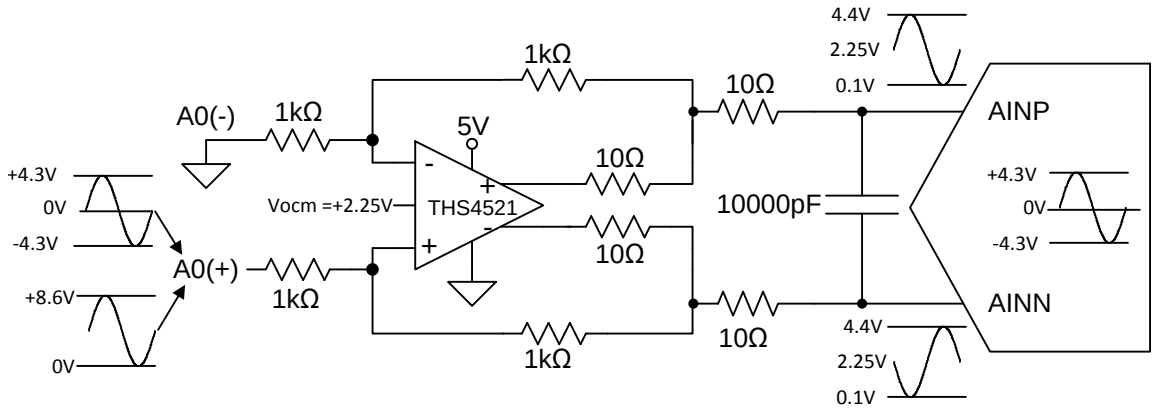


Figure 2. Single-Ended Signal Example

2.3 Voltage Reference

The reference voltage should be below 5 V because the EVM is powered by a 5-V analog supply. This EVM uses a 4.5 V value created by the onboard REF5045. This value is then filtered by an RC filter with a 160-Hz cutoff frequency to minimize noise contribution. Finally, the filtered reference value is buffered by the THS4281 that functions as the driver for the ADC reference input pin. To meet performance specifications, a 10-µF capacitor with a small ESR is also present at the ADC reference input pin. This large capacitive load reduces the THS4281 effective bandwidth to 2 MHz, making the THS4281 total noise contribution approximately 22 μ_{VRMS}. The OPA333 and the additional feedback are optional, but do complement the THS4281 by minimizing offset and drift.

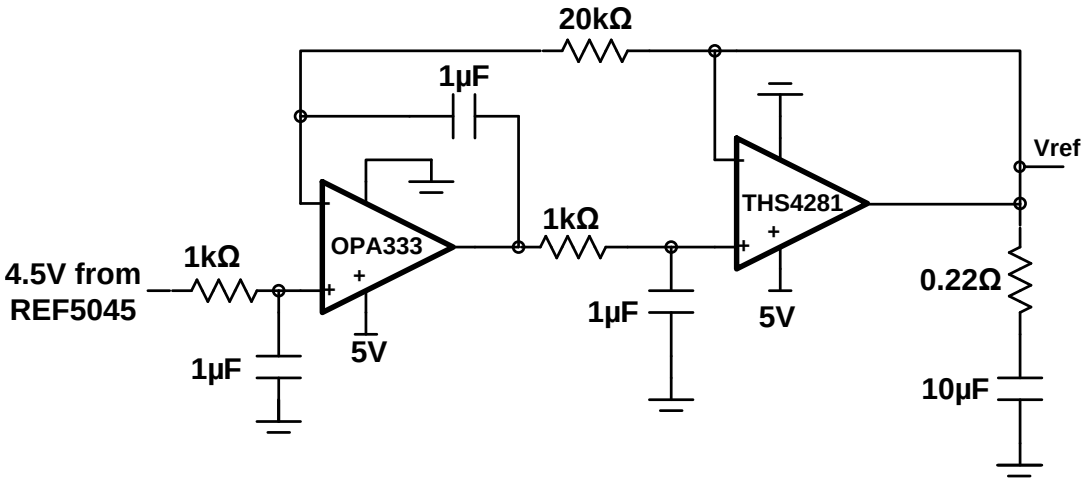


Figure 3. THS4281 Reference Driver with Complementary OPA333 for Drift and Offset Correction

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3 EVM Digital Interface

Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-L-DV-P provide convenient 10-pin, dual-row, header and socket combinations at P1. The header and socket provides access to the ADC digital control pins. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 3 summarizes the pinouts for the digital interface J2.

Table 3. J2: Serial Interface Header

Pin Number	Signal	Description
J2.1	$\overline{CS}$ or CONVST	Chip-select input that can be used as a convert start
J2.3	SCLK	Serial clock input
J2.7	$\overline{CS}$ or CONVST	Chip-select input that can be used as a convert start intended for the MMB0 motherboard
J2:13	SDO or MISO	SDO or MISO output
J2.15	INT	20-kΩ pull-up resistor for detecting falling edges at the end of conversions
J2.17	CONVST	Directly connects to the convert start pin if JP3 is installed
J2.4, J2.10, and J2.18	GND	Digital ground connections
J2.16, J2.20	I^2C™ bus	I^2C bus; used only used to program the U4 EEPROM on the EVM board
J2.2, J2.5-6, J2.8-9, J2.11-12, J2.14, and J2:19	Unused	Unused

3.1 Serial Interface (SPI)

The ADS8861 ADC uses SPI serial communication in mode 1 (CPOL = 0, CPHA = 1) with high-speed clocks greater than 30 MHz or uses mode 0 (CPOL = 0, CPHA = 0) for slower clocks. Because the serial clock (SCLK) frequency can be as fast as 80 MHz, the ADS8861EVM offers 47-Ω resistors between the SPI signals and J2 to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 47-Ω resistors slow down the signal edges in order to minimize signal overshoot.

3.2 I^2C Bus for Onboard EEPROM

The ADS8861EVM has an I^2C bus that records the board name and assembly date to communicate with the onboard EEPROM. This bus is not used in any form by the ADS8861 converter.

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4 EVM Power-Supply Inputs

J3 is the power-supply input connector. Table 4 lists the configuration details for J3.

Table 4. J3: Power-Supply Interface Header

Pin Number	Pin Name	Function	Required
J3.3	+5VA	5-V analog supply	Yes
J3.5	GND	Digital ground input	Yes
J3.6	GND	Analog ground input	Yes
J3.7	1.8 VD	1.8-V digital supply	Optional
J3.9	3.3 VD	3.3-V digital supply	Yes
J3.10	5 VD	5-V digital supply	No
P3.1-2, P3.4, and P3.7-8	Unused	Unused	No

4.1 Analog Power Options

The ADS8861EVM board is designed to function with a 5-V analog power supply connected to J3.3. The ADS8861 is limited to 3.6 V as an analog supply. Therefore, the board regulates down the 5-V analog supply with an onboard 3.3-V LDO (TPS78833).

4.2 Digital Power Options

The ADS8861EVM connects the digital power supply of the ADS8861 to 3.3 VD (J3.10) with a 0-Ω resistor. This 3.3-V supply matches the 3.3-V logic level of the MMB0 motherboard.

4.3 Analog and Digital Grounds

The EVM only has one ground plane for analog and digital supplies; thus, pins J3.5 and J3.6 are tied together to this ground plane. Therefore, both supply grounds should be connected to pins J3.5–6 in order to share the same ground.

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5 EVM Digital Configuration

The EVM offers two jumpers (JP2 and JP3) to configure the EVM in either 3-wire or 4-wire SPI mode. By default, the EVM jumper settings are 3-wire. JP1 only establishes the pin that carries the chip-select signal from the J2 header.

5.1 SPI 3-Wire Mode (JP2:2–3 and JP3:OPEN)

The chip-select signal is used to bring the ADS8861 digital output out of 3-state and initialize conversions. The rising edge of the chip-select signal starts a conversion, then after the conversion time the falling edge of chip-select brings the digital output out of 3-state. Figure 4 shows this configuration.

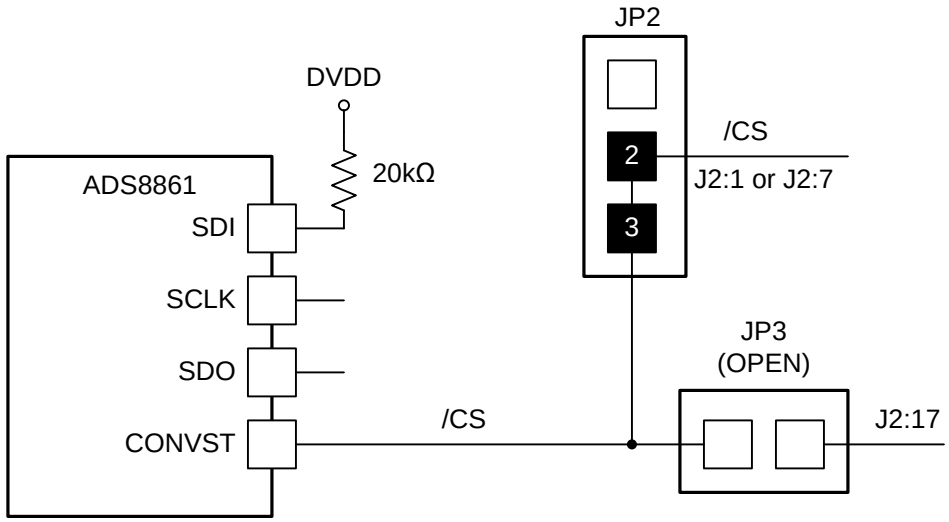


Figure 4. Serial 3-Wire Configuration

5.2 SPI 4-Wire Mode (JP2:1–2 and JP3:CLOSED)

The chip-select signal is used to bring the ADS8861 digital output out of 3-state. However, conversion is initialized from J3:17 as an independent signal. The rising edge of J3:17 (CONVST) starts a conversion, then after the conversion time the falling edge of the chip-select brings the digital output out of 3-state. Figure 5 shows this configuration.

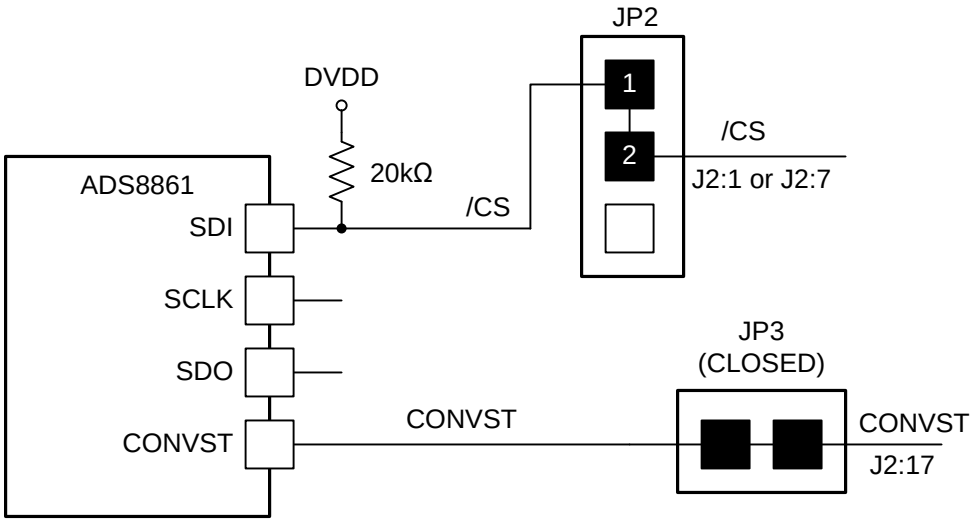


Figure 5. Serial 4-Wire Configuration

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6 PDK Kit Setup

NOTE: Do not connect the ADS8861EVM-PDK to a computer before completing Section 6. Failure to observe this caution may cause Microsoft Windows to disregard the ADS8861EVM-PDK as a connected device.

This section presents the steps required to setup the ADS8861EVM-PDK kit before operation.

Section 7 explains how to operate the kit to acquire and analyze data.

The steps to setup the kit are as follows and must be completed before attempting to capture data:

Step 1. Download and install the ADCPro software (if not already installed) to a computer.

Step 2. Download and install the ADS8861EVM-PDK EVM plug-in software.

Step 3. Configure the ADS8861EVM-PDK hardware.

Step 4. Power-up the ADS8861EVM-PDK.

Each task is described in the subsequent sections of this document.

6.1 Installing the ADCPro Software

ADCPro is the primary program used to evaluate the ADS8861. ADCPro is available for download at www.ti.com/tool/adcpro. Refer to the *ADCPro User's Guide* (SBAU128) for detailed installing instructions.

6.2 Installing the ADS8861EVM-PDK Plug-In Software

NOTE: ADCPro should be installed before attempting to install the ADS8861EVM-PDK plug-in software.

The installation file link for the PDK plug-in can be found in the ADS8861EVM-PDK product folder at www.ti.com/tool/ads8861evm-pdk. In the software section, look for a link with a file named **ads886x-adcproplugin-<version #>.exe** (<*version* #> refers to the installation file version number, and increments with software version releases). Download and double-click the file to run it; then follow the instructions as shown.

Figure 6 shows the initial and completed installer screen shots, respectively.

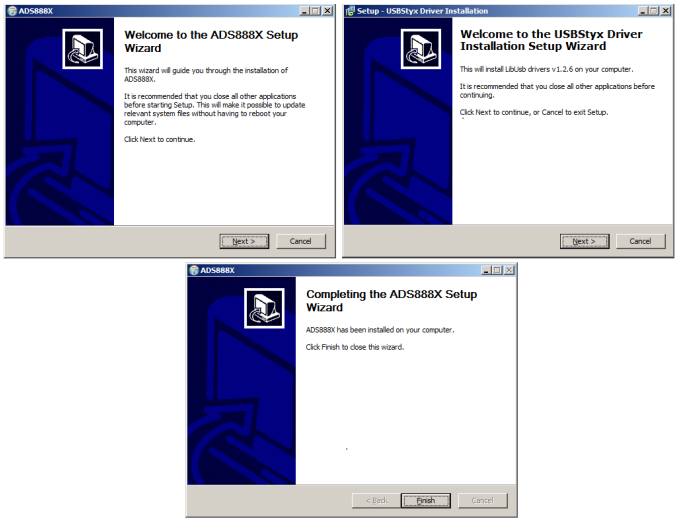


Figure 6. Plug-In Installer

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6.3 Configuring the ADS8861EVM-PDK Hardware

The ADS8861EVM-PDK contains both the ADS8861EVM and the MMB0 motherboard; however, the devices may be shipped unconnected or configured incorrectly. Follow these steps to verify that the ADS8861EVM-PDK kit is properly configured and connected.

Step 1. Unpack the ADS8861EVM-PDK kit.

Step 2. Set J12 to closed, J13A to open, and J13B to closed on the MMB0, as shown in Figure 7.

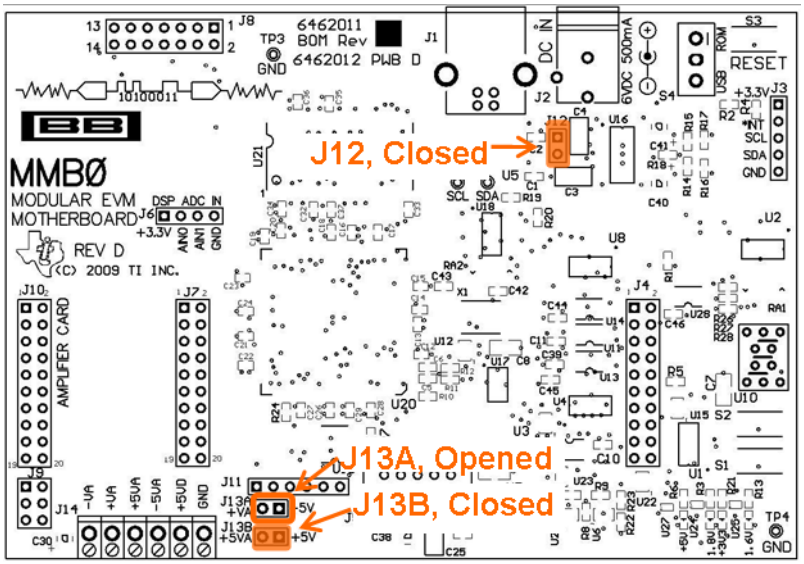


Figure 7. MMB0 Motherboard Jumper Configuration

- J12 must be closed. This setting allows the wall supply to power-up the MMB0 and the ADS8861EVM through J2 (6-VDC input), and regulate down to 5 V, 3.3 V.
- J13B must be closed. This setting connects the 5-V analog power supply with the 5-V digital power supply.
- J13A must be opened. This setting allows the 5-V analog power supply to be regulated onboard.

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3. Set JP1:2–3, JP2:2–3, and JP3:open on the ADS8861EVM, as shown in Figure 8.

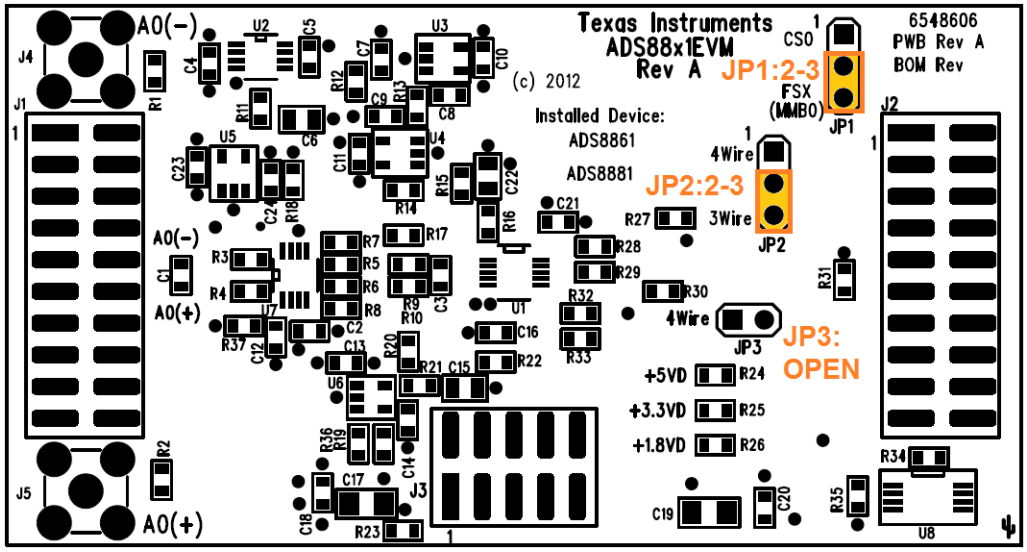


Figure 8. ADS8861EVM Jumper Configuration

Step 3. Plug the ADS8861EVM into the MMB0.

CAUTION

To avoid bending the connector pins and damaging the EVM, do not misalign the pins when plugging the ADS8861EVM into the MMB0. Check the pin alignment carefully before applying power to the PDK.

6.4 Powering up the ADS8861EVM-PDK

When the ADS8861EVM-PDK kit is configured, power can be applied to the MMB0. This power comes from a wall supply that delivers 6 VDC to the MMB0 through J2 on the MMB0 motherboard. This wall power supply is included with the PDK.

After the power supply is connected, four green light-emitting diodes (LEDs) in the bottom right-hand corner of the MMB0 motherboard should light up. If these LEDs do not light up, disconnect the power and verify that J12 is closed on the MMB0 motherboard.

7 PDK Kit Operation

The evaluation software is based on ADCPro. This program operates using a variety of plug-ins. To use ADCPro, load an EVM plug-in and a test plug-in (select them from the EVM and Test menus, respectively). To unload a plug-in, select the Unload option from the corresponding menu.

The following sections describe how to use ADCPro and the ADS8861EVM plug-in to acquire data.

7.1 About MMB0

The MMB0 provides the USB interface between the computer and the ADS8861EVM. The MMB0 is a modular EVM system motherboard designed around the TMS320VC5509, a DSP with an onboard USB interface from Texas Instruments. The MMB0 also has 16 MB of SDRAM installed.

The MMB0 is not sold as a DSP development board, and is not available separately. TI cannot offer support for the MMB0 except as part of an EVM kit. For schematics or other information about the MMB0, contact Texas Instruments.

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7.2 Loading the ADS8861EVM-PDK Plug-in

Step 1. Make sure the PDK kit is configured and powered up as explained in Section 6. Then, press the **Reset** button on the MMB0 (in the top right-hand corner) one time to clear board memory.

Step 2. Connect the MMB0 to a computer using the USB cable provided with the kit.

Step 3. Start ADCPro from the Windows *Start* menu.

Step 4. Load the ADS886XEVM plug-in from the ADCPro drop-down *EVM* menu, as shown in Figure 9. Note that only one EVM plug-in can be loaded at a time. If a different plug-in is selected, the previous plug-in is unloaded.

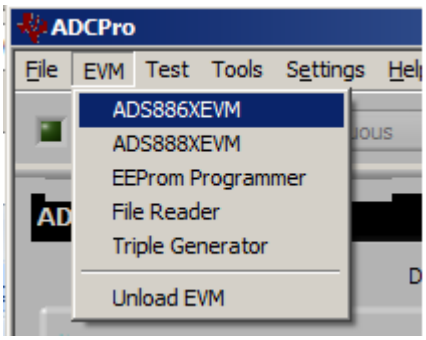


Figure 9. Loading EVM Plug-in

Step 5. When the plug-in is loaded, the plug-in searches for the board. A series of messages in the status area indicates this action, eventually showing *Connected to EVM*.

The plug-in is now loaded and ready to function with the ADS8861EVM.

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7.3 Using the ADS8861EVM Plug-in

The ADS8861EVM allows the user to evaluate the ADS8861 ADC. Figure 10 shows the device configuration tab of the ADS8861EVM plug-in that is used to change acquisition parameters such as sample rate and voltage reference.

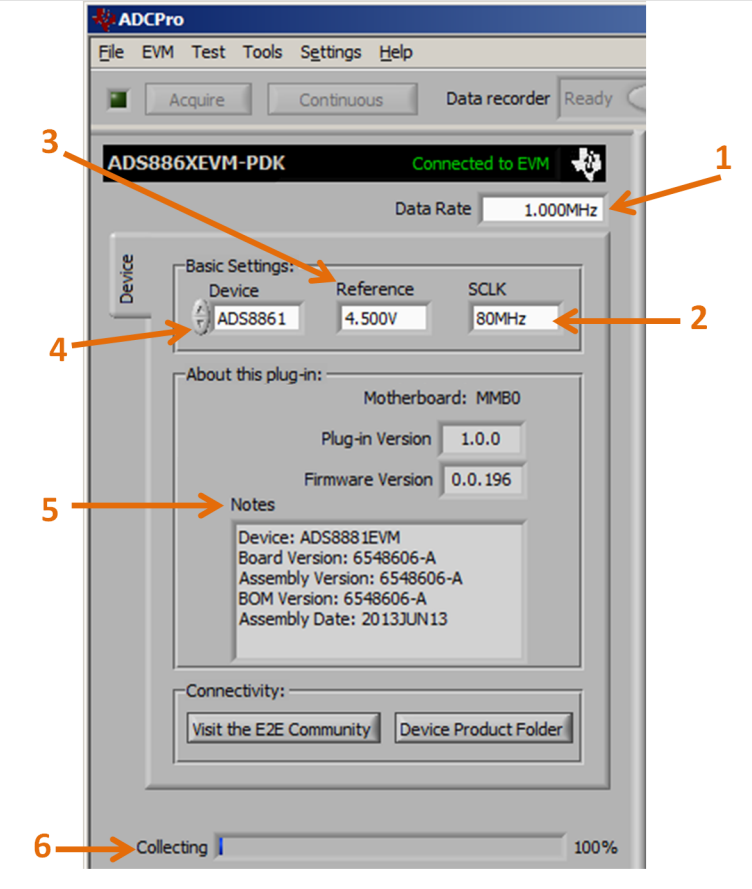


Figure 10. ADS8861EVM Plug-In: Device Configuration Tab

The device configuration tab contains the following controls:

- **Data rate:** By default, data rate is 1 MSPS. This control shows the data rate or sampling frequency used by the ADC to acquire data. With an SCLK frequency of 80 MHz, data rate can be set from 19.536 kSPS to 1 MSPS. With an SCLK frequency of 10 MHz, data rate can be set from 4 kSPS to 344.827 kSPS.
- **SCLK:** By default, SCLK is 80 MHz. SCLK sets the clock frequency used by the SPI interface to capture data. SCLK should be between 70 MHz to 80 MHz for 1 MSPS. For slow sampling rates, use 10 MHz. Do not use SCLK frequencies between 30 MHz and 50 MHz.
- **Reference:** 4.5 V is the default reference value, which matches the onboard reference of the EVM. The value of this control should always match the reference used by the ADC to read accurate voltages.
- **Device selection:** The ADS8861 is selected by default.
- **About:** This control shows the motherboard name, plug-in version, firmware version, assembly date, and board revision information. Note that the device name displayed is ADS8881 instead of ADS8861 because the main software is based on the ADS8881 device.
- **Collection bar:** This feature shows the percentage of data collected during an acquisition session.

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7.4 Loading the Test Plug-in

When the ADS8861EVM plug-in is configured, one of the four test plug-ins must be loaded to acquire data using the drop-down Test menu, as shown in Figure 11. Note that only one Test plug-in can be loaded at a time. If a different plug-in is selected, the previous plug-in is unloaded.

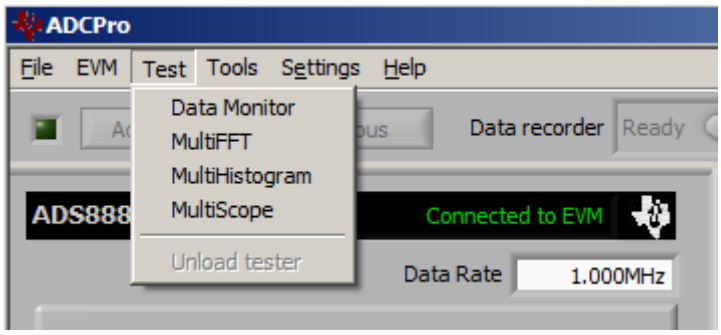


Figure 11. ADCPro Test Plug-ins

There are four different test options available for the ADS8861EVM:

- **Data monitor:** This test option acquires and exports data in table format as hexadecimal data.
- **MultiFFT:** This test option allows the user to acquire data and create an FFT graph of power versus frequency to display data.
- **MultiHistogram:** This test option acquires data and creates a histogram of code values.
- **MultiScope:** This feature acquires and displays data in a graph of voltage versus time.

For further details regarding how to set up and use the various test plug-ins, refer to the *ADCPro User's Guide* (SBAU128).

7.5 Acquiring Data

When the ADS8861EVM is configured for the desired test scenario, press the **Acquire** button to start the data collection process; the software collects the number of data points specified in the *Test* plug-in **Block Size** control. While acquiring data, the ADS8861EVM plug-in disables all front panel controls, and the collection process bar displays the completion progress.

7.6 Troubleshooting

If the ADS8861EVM plug-in cannot find the ADS8861EVM-PDK, press the **RESET** button on the MMB0 and try again.

If ADCPro stops responding while the ADS8861EVM-PDK is connected, shut down and restart the ADCPro software. Also, try unplugging the USB cable from the PDK.

8 Bill of Materials, Schematics, and Layout

The bill of materials is provided in Table 5. Section 8.2 illustrates the PCB layouts for the ADS8861EVM. The schematic is illustrated in Figure 16.

8.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, refer to www.ti.com.)

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Table 5. ADS8861EVM Bill of Materials

Item No.	Qty	Value	Ref Des	Description	Manufacturer	Part Number
1	1	—		Printed Circuit Board, 3.2 in x 1.7 In. x 0.062 in.	Texas Instruments	6548606
2	1	—	C1	Not Installed	—	—
3	5	0.1 µF	C2, C10, C11, C14, C23	Capacitor, X7R Ceramic ±10%, 25WV, 0603	Murata	GRM188R71E104KA01D
4	1	10000 pF	C3	Capacitor, NP0 Ceramic ±5%, 50WV, 0603	TDK	C1608C0G1H103J
5	9	1 µF	C4, C5, C7-C9, C12, C13, C21, C24	Capacitor, X7R Ceramic ±10%, 25WV, 0603	Murata	GRM188R71E105KA12D
6	3	10 µF	C6, C15, C22	Capacitor, X7R Ceramic ±10%, 10WV, 0805	Murata	GRM21BR71A106KE51L
7	3	1000 pF	C16, C18, C20	Capacitor, C0G Ceramic ±5%, 50WV, 0603	Murata	GRM1885C1H102JA01D
8	2	10 µF	C17, C19	Capacitor, X7R Ceramic ±10%, 16WV, 1206	TDK	C3216X7R1C106K
9	2	—	J1, J2 (Top)	Header 20 Pin SMT Plug, .100" Gold (2x10)	Samtec	TSM-110-01-L-DV-P
10	2	—	J1, J2 (Bottom)	Header 20 Pin SMT Socket, .100" Gold (2x10)	Samtec	SSW-110-22-F-D-VS-K
11	1	—	J3 (Top)	Header 10 Pin SMT Plug, .100" Gold (2x5)	Samtec	TSM-105-01-L-DV-P
12	1	—	J3 (Bottom)	Header 10 Pin SMT Socket, .100" Gold (2x5)	Samtec	SSW-105-22-F-D-VS-K
13	2	—	J4, J5	CONN SMA JACK STRAIGHT PCB	Amphenol	132134
14	2	—	JP1, JP2	Header Strip, 3 pin .100" Gold (1x3)	Samtec	TSW-103-07-L-S
15	1	—	JP3	Header Strip, 2 pin .100" Gold (1x2)	Samtec	TSW-102-07-L-S
16	7	—	R1, R2, R20, R24, R26, R34, R36	Not Installed	—	—
17	4	1k	R3, R4, R5, R6	Resistor, Thin Film Chip, 0.1%, 1/10W, 0603	Panasonic	ERA-3AEB102V
18	5	10	R7-R10, R22	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Vishay/Dale	CRCW060310R0FKEA
19	3	0.22	R11, R16, R21	Resistor, Thin Film Chip, 1%, 1/5W, 0603	Susumu	RL0816S-R22-F
20	3	1k	R12, R13, R37	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1001V
21	5	0	R14, R19, R23, R25, R30	Resistor, Thick Film Chip, 1/10W, 0603	Panasonic	ERJ-3GEY0R00V
22	5	20k	R15, R17, R18, R27, R31	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF2002V
23	5	47	R28, R29, R32, R33, R35	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF47R0V
24	1	—	U1	IC ADC 16-bit 1MSPS Fully Diff 10-MSOP	Texas Instruments	ADS8861IDGS
25	1	—	U2	IC VREF SERIES PREC 4.5V 8-MSOP	Texas Instruments	REF5045IDGK
26	1	—	U3	IC OPAMP CHOP R-R 350KHZ SOT23-5	Texas Instruments	OPA333AIDBV
27	1	—	U4	IC OPAMP VFB R-R 95MHZ SOT23-5	Texas Instruments	THS4281DBV
28	1	—	U5	IC OPAMP GP R-R CMOS SOT23-5	Texas Instruments	OPA330AIDBV
29	1	—	U6	IC REG LDO 3.3V .15A SOT-23-5	Texas Instruments	TPS78833DBV
30	1	—	U7	IC OPAMP DIFF R-R 145MHZ 8MSOP	Texas Instruments	THS4521IDGK
31	1	—	U8	IC EEPROM 256KBIT 400KHZ 8TSSOP	Microchip	24LC256-I/ST
32	2	—	—	0.100 Shunt - Black Shunts	3M	969102-0000-DA

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8.2 Board Layouts

Figure 12 through Figure 15 show the PCB layouts for the ADS8861EVM.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; these figures are not intended to be used for manufacturing ADS8861EVM PCBs.

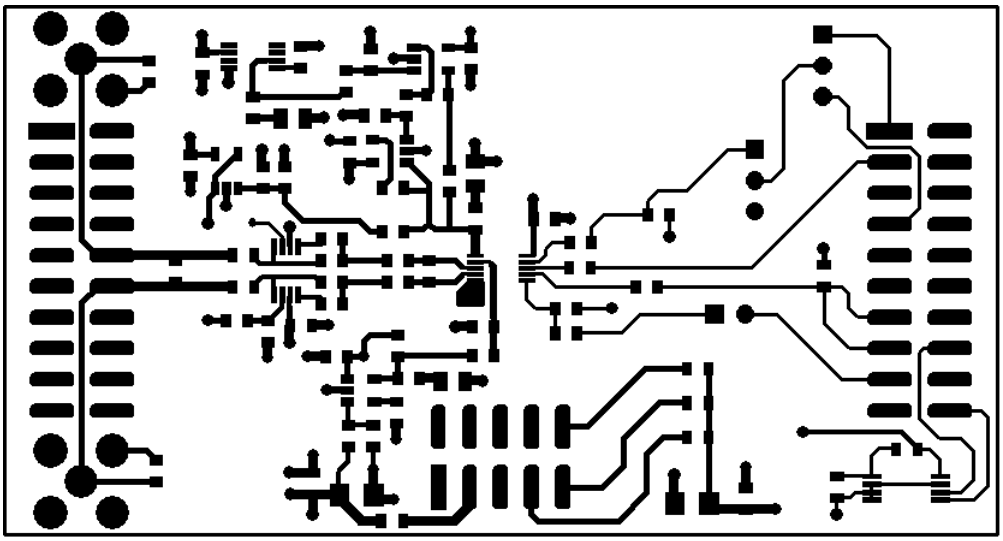


Figure 12. ADS8861EVM PCB: Top Layer

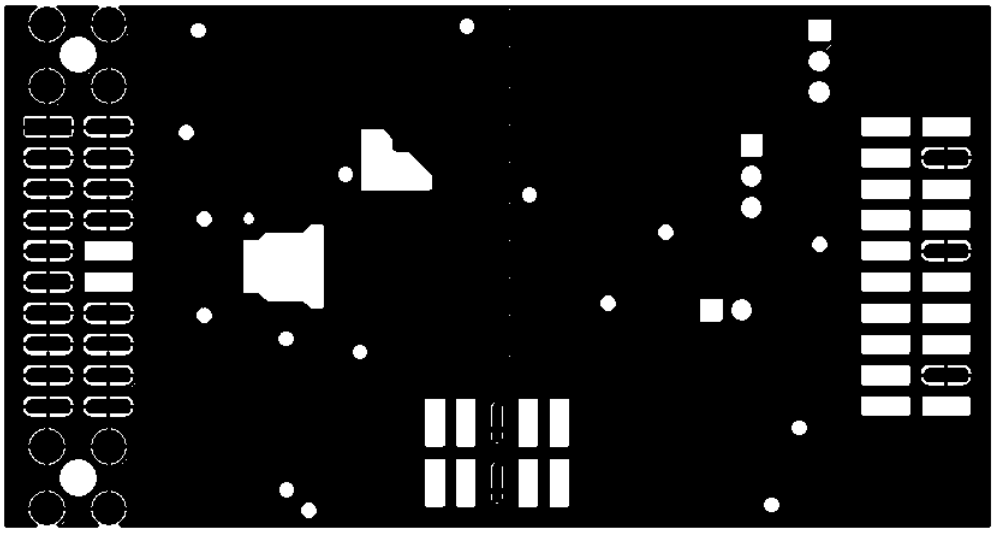


Figure 13. ADS8861EVM PCB: Ground Layer

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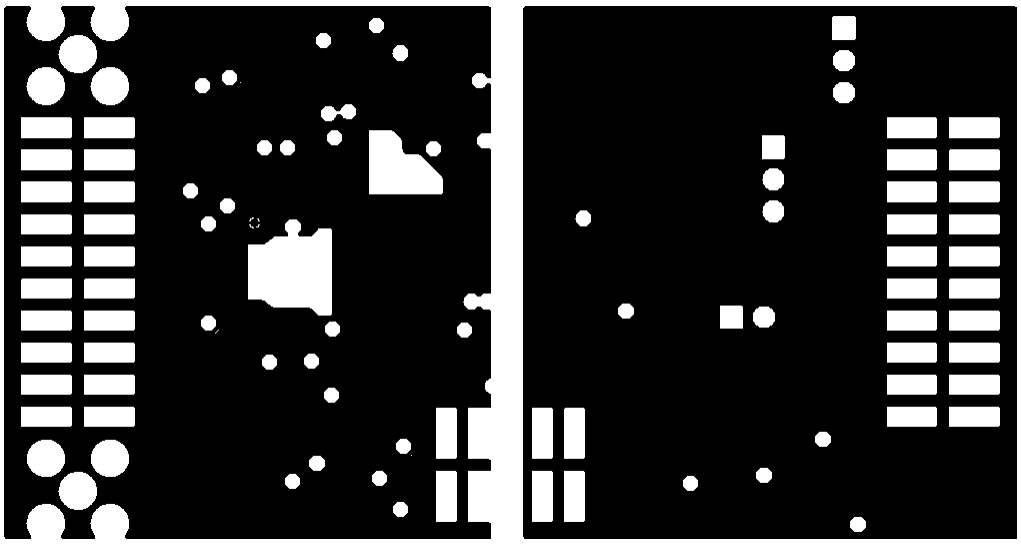


Figure 14. ADS8861EVM PCB: Power Layer

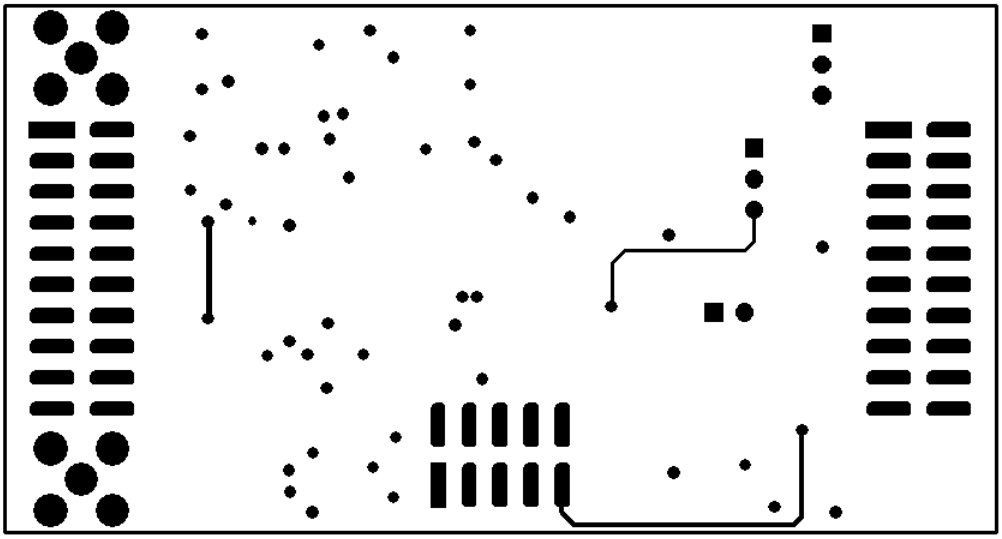


Figure 15. ADS8861EVM PCB: Bottom Layer

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8.3 Schematic

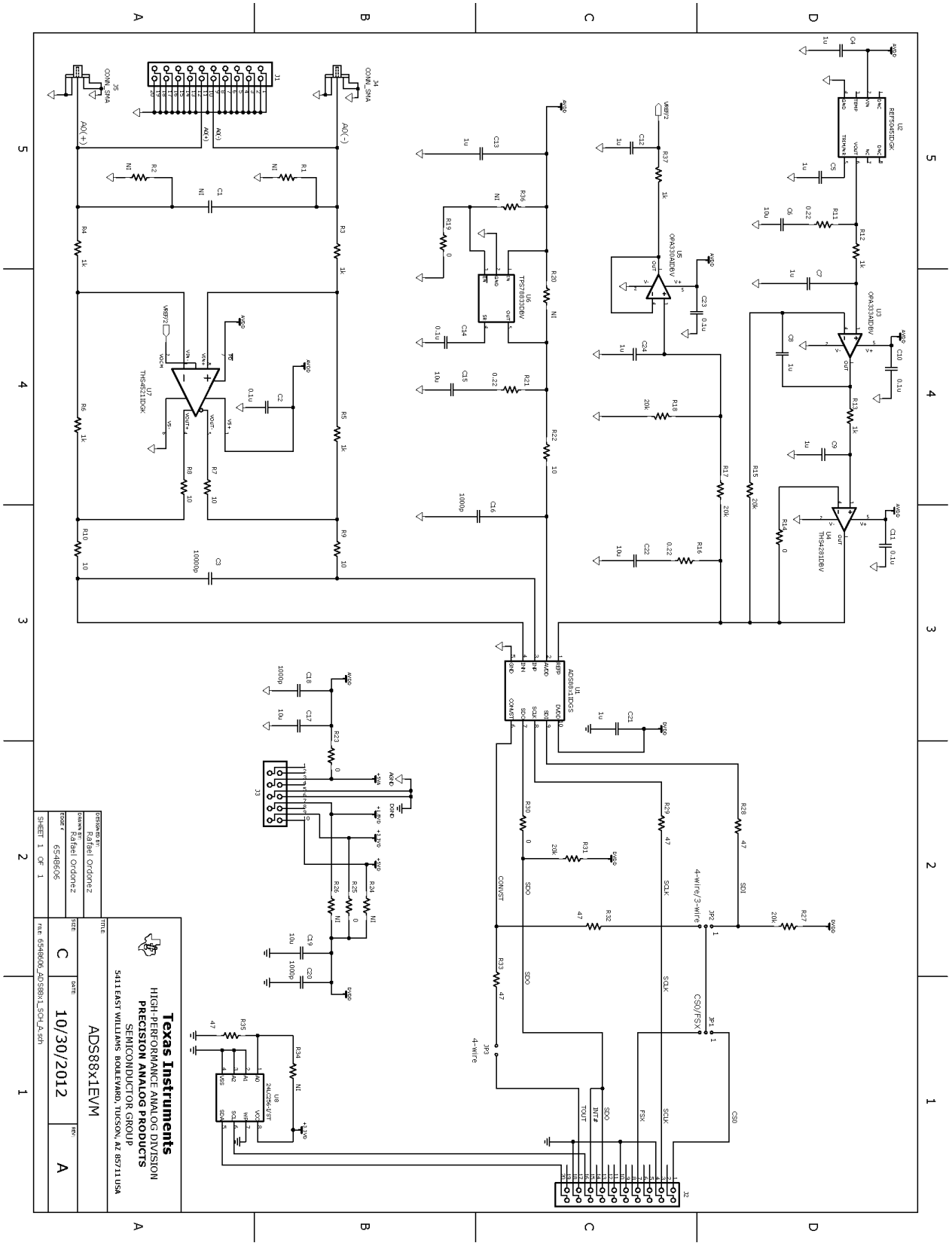


Figure 16. ADS8861EVM Schematic

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Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than . The EVM is designed to operate properly with certain components above as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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